IDEC Chip Design Contest

A 10-bit Parasitic Capacitance Insensitive SAR ADC using Custom Routing Capacitor

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Introduction

Arrive of the Internet of Things(IoT) era, these days wireless sensor networks (WSNs) are uses variety in daily life. WSN application requires low power consumption and smaller size. As a result, the consumption of high-performance low-power analog-to-digital converter (ADC) is also increasing.

Since CDAC consumes a lot of power and affects to the performance of the entire ADC, various structures have been proposed and studied.

BWA capacitive array is a structure that reduces the total capacitance by dividing the capacitor array into k MSBs and m = N-k LSBs using an attenuation capacitor.

The advantage of the BWA capacitive array is that the total capacitance is small than CBW so power consumption also can be reduced.

However, it is more sensitive to mismatch of capacitor than CBW capacitive array. Affection of mismatch can express by INL and DNL.

Proposed CDAC Layout Technique

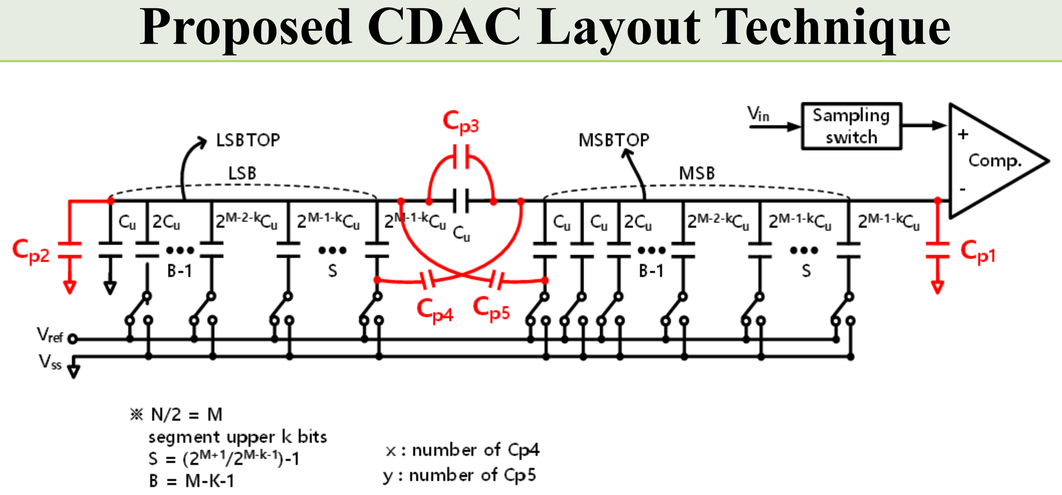

Figure 1. Schematic of SAR ADC with segment BWA DAC and parasitic capacitor

To relieve effect of mismatch and parasitic capacitance, segment BW DAC structure is used. The upper k bits of each LSB and MSB of the BWA DAC structure are segmented. When using the segment BWA DAC structure, the parasitic capacitance that occurs during layout greatly affects the linearity. Fig.1. shows the parasitic that can occur in the segment BWA DAC.

MSBTOP to VSS (C_{p1}) reduce the input voltage range. It does not degraded linearity. On the other hand, LSBTOP to VSS (C_{p2}) is not constant with input changing so it degrades ADCs linearity.

MSBTOP to LSBBOT (C_{p4}) makes LSBBOT switching affects to MSBTOP voltage. And MSBBOT to LSBTOP (C_{p5}) makes LSBBOT switching affects to the MSBTOP voltage. To eliminate and reduce these parasitic capacitors, a layout technique has been proposed. The layout technique was proposed to eliminate the two parasitic capacitances for improving linearity of SAR ADC.

Using a custom routing capacitor is proposed to eliminate MSBTOP to LSBBOT (C_{p4}) and MSBTOP to LSBTOP (C_{p3}).

Two types routing capacitor are needed to connect the attenuation capacitor and the MSB and LSB array. These two routing capacitors are used to connect the top plate of the attenuation to the top plate of the capacitor array, and the bottom plate of the attenuation and the bottom plate of the capacitor array.

There are two possible cases of deploying two routing capacitors. First case, the bottom plate of attenuation capacitor and MSBTOP is connected by using TOP to BOT routing capacitor and top plate of attenuation capacitor is connected to LSBTOP by TOP to TOP routing capacitor.

The second case of CDAC layout, the top plate of attenuation capacitor in case-2 is connected to MSBTOP and bottom plate is connected to LSBTOP. Two additional parasitic capacitances are also generated in the case 2 as shown in Fig. 10. The size of LSBTOP to VSS (C_{p2}) is 8.33 fF. This value is 71.4% less than case-2. But the capacitance of MSBTOP to VSS (C_{p1}) parasitic capacitor increased. Since MSBTOP to VSS (C_{p1}) parasitic capacitor does not affects to linearity, the case-2 layout is finally selected for the proposed scheme.

As a result, 10-bit SAR ADC without routing capacitor and with routing capacitor in case-2 are fabricated to validate proposed layout technique. CDAC array layout is shown in Fig. 3.Core size of SAR ADC is 283 um × 270 um. It is designed compactly to maintain the advantage of SAR ADC.

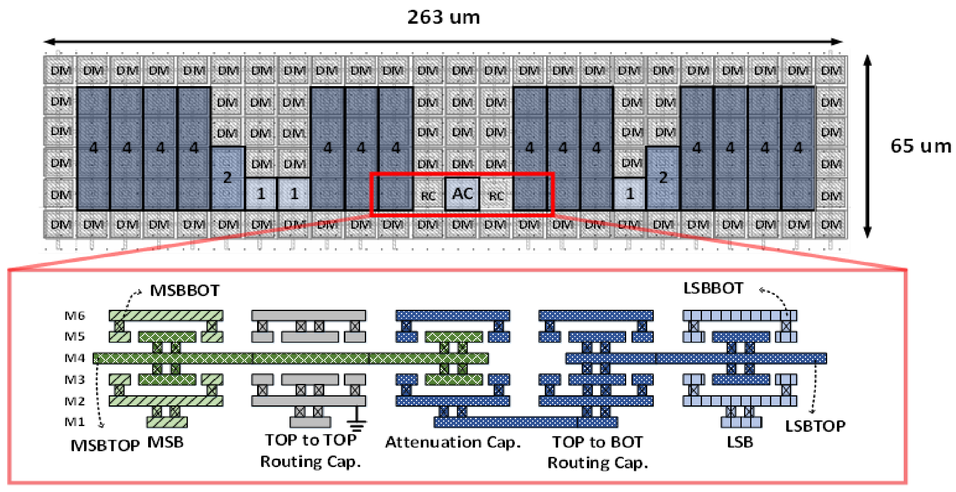

Figure 3. CDAC array with proposed layout technique

Conclusion

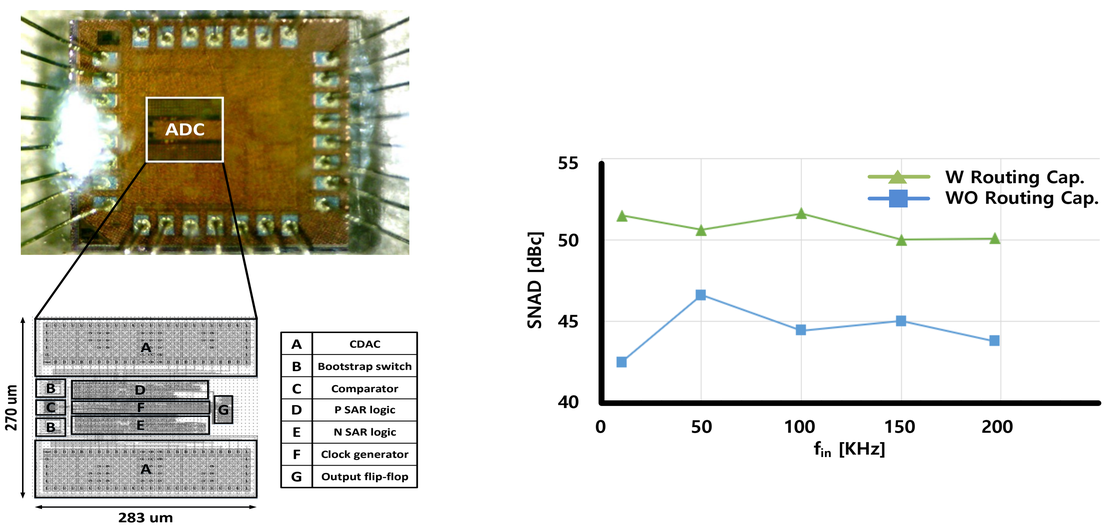

Figure 4. (a) Die photo and layout of the SAR ADC with proposed layout technique, (b) Dynamic performance of with and without proposed technique

	Segment BWA DAC WO. routing cap.	Segment BWA DAC W. routing cap.
Technology (nm)	65	65
Supply voltage (V)	1.2	1.2
Sampling Freq. (S/s)	400K	400K
Resolution (bit)	10	10
Unit Cap. (F)	22.17 f	22.17 f
INL* (LSB)	+ 1.25/- 1.22	+ 0.3/- 0.06
DNL* (LSB)	+ 1.43/- 0.04	+ 0.1/- 0.13
SNDR (dB) @f_{in}=10K	44.92	51.48
ENOB** (bits)	7.5	8.02

* Simulation result
** Effective number of bits

Figure 5. Performance summary

The prototype with proposed layout technique is fabricated by using 65nm CMOS technology. The results shows the performance improvement compared to without using proposed technique. Effects of parasitic capacitance is analyzed to improve linearity. Through the analysis it is confirmed that four types of major parasitic capacitor affect to linearity. These parasitic capacitors can be reduced degrading linearity by using custom routing capacitor.

Acknowledgement

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.